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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
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Katsumi SHIBAYAMA	)	Confirmation No.: 1521
	)	
Application No.: 10/668,605	)	Group Art Unit: 2811
	)	
Filed: September 24, 2003	)	Examiner: Not Yet Assigned
	)	
For: PHOTODIODE ARRAY AND METHOD OF MAKING SAME	)	

Commissioner for Patents
Arlington, VA 22202

Sir:

SUBMISSION OF TRANSLATION OF
PRIOR-FILED PROVISIONAL APPLICATION

Applicant attaches hereto an English translation of U.S. Provisional Application No. 60/430,674, to which priority is claimed in the above-identified patent application. This Japanese language document was filed in the U.S. Patent and Trademark Office on December 4, 2002. The declaration of Mr. Shiro Terasaki attached to the translation constitutes a statement that the translation is accurate in accordance with 37 C.F.R. § 1.78(5)(iv) and MPEP § 201.11.

Applicant believes that no fees are due in connection with the filing of this paper. However, if there are any fees due in connection with the filing of this paper, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under

37 C.F.R. § 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

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[Document Name] Specification

[Title of the Invention]

Photodiode Array and Method of Making the Same

[Claims]

1. A photodiode array comprising:

a semiconductor substrate of a first conduction type formed with an array of a plurality of pn junction type photodiodes on an incident surface side for light to be detected, the surface opposite from the incident surface in the semiconductor substrate being made of a (100) plane;

a through hole, formed in an area held between the photodiodes, penetrating through the semiconductor substrate from the incident surface side to the opposite surface side; and

a conductive layer extending from the incident surface to the opposite surface by way of a wall surface of the through hole,

wherein said through hole is formed by connecting, within the semiconductor substrate, a vertical hole part formed substantially perpendicular to the incident surface on the incident surface side and a pyramidal hole part formed like a quadrangular pyramid on the opposite surface side,

and the pyramidal hole part has a wall surface formed as a (111) plane.

2. A photodiode array according to claim 1, further comprising a high impurity concentration layer of the first conduction type surrounding the through hole within the semiconductor substrate.

3. A method of making a photodiode array, the method comprising:

a first step of preparing a semiconductor substrate having a first surface formed as a (100) plane, and forming a predetermined area of a second surface opposite from the first surface with an array of a plurality of pn junction type photodiodes;

a second step of forming a pyramidal depression having a quadrangular pyramid form with a depth smaller than a thickness of the semiconductor substrate from the first surface side of the semiconductor substrate by anisotropic etching for the plurality of photodiodes;

a third step of forming a vertical hole substantially perpendicular to the second surface by dry etching from the second surface side at a position corresponding to the pyramidal depression, and connecting the pyramidal depression to the vertical hole, so as to form a through hole penetrating through the semiconductor substrate from the second surface to the first surface; and

a fourth step of forming a conductive layer

extending from the second surface to the first surface by way of the through hole.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention Pertains]

The present invention relates to a photodiode array and a method of making the same.

[0002]

[Prior Art]

Photodiode arrays for CT have been required to have a larger area. For eliminating insensible regions from a photodiode array, three-dimensional packaging is necessary, in which a signal processing unit is disposed on the opposite side (rear side) of the light incident surface. To this aim, it is necessary for an electrode formed on the incident side (front side) by using a through hole wiring to be drawn to the opposite side (rear side) of the incident surface. Semiconductor devices using such a through hole wiring are disclosed, for example, in Japanese Patent Application Laid-Open No. HEI 5-29483 and Japanese Patent Application Laid-Open No. HEI 6-177201. In the semiconductor device disclosed in Japanese Patent Application Laid-Open No. HEI 5-29483, a wet etching with an alkali solution is used n order to form a

through hole, whereby the revealed plane of substrate is at an angle of 54.7° with respect to the substrate surface.

[0003]

Patent Document 1: Japanese Patent Application Laid-Open No. HEI 5-29483

Patent Document 2: Japanese Patent Application Laid-Open No. HEI 6-177201

[Problem to be Solved by the Invention]

[0004]

When forming an electrode of each of photodiodes in a photodiode array by using the technique mentioned above, however, the through hole gradually increases its width from the front side to the rear side. Therefore, the photodiodes cannot be formed so close to each other, whereby the filler is limited. Further, as shown in Fig. 14, the angle θ formed between the surface on the front side of the substrate and the inner wall surface of the through hole becomes acute. Therefore, if the acute corner 20 is covered with a through hole wiring 17, conduction is likely to fail at the part of corner 20 because of insufficient coverage with the wiring.

[0005]

Though dry etching may be used for forming a through hole perpendicular to the substrate surface,

it is practically impossible to form a through hole with a uniform diameter in a substrate having a thickness of 250 to 400 μm. Also, since the processing rate of dry etching is low, it takes a long processing time to penetrate through the substrate having a thickness of 250 to 400 μm.

[0006]

Hence, it is an object of the present invention to overcome the problem mentioned above and provide a photodiode array which is less likely to cause conduction failures in through hole wirings, while yielding a large fill factor.

[0007]

[Means for Solving the Problem]

For overcoming the above-mentioned problem, the present invention provides a photodiode array comprising: a semiconductor substrate of a first conduction type formed with an array of a plurality of pn junction type photodiodes on an incident surface side for light to be detected, the surface opposite from the incident surface in the semiconductor substrate being made of a (100) plane; a through hole, formed in an area held between the photodiodes, penetrating through the semiconductor substrate from the incident surface side to the opposite surface side; and a conductive layer extending from the

incident surface to the opposite surface by way of a wall surface of the through hole, wherein the through hole is formed by connecting, within the semiconductor substrate, a vertical hole part formed substantially perpendicular to the incident surface on the incident surface side and a pyramidal hole part formed like a quadrangular pyramid on the opposite surface side, and the pyramidal hole part has a wall surface formed as a (111) plane.

[0008]

In this photodiode array, all the covering corners' angles of the conductive layer extending from the incident surface to the opposite surface by way of the wall surface of the through hole become 90° or greater, whereby conduction failures are less likely to occur because of insufficient coverage with the conductive layer. Also, even when the photodiodes are disposed close to each other, the fill factor can be increased.

[0009]

The photodiode array in accordance with the present invention may further comprise a high impurity concentration layer of the first conduction type surrounding the through hole within the semiconductor substrate.

[0010]

This photodiode array comprises the high impurity concentration layer surrounding the through hole, and thus can trap unnecessary carriers which may occur when the through hole is mechanically damaged, thereby suppressing leak currents and dark currents.

[0011]

The present invention provides a method of making a photodiode array comprising: a first step of preparing a semiconductor substrate having a first surface formed as a (100) plane, and forming a predetermined area of a second surface opposite from the first surface with an array of a plurality of pn junction type photodiodes; a second step of forming a pyramidal depression having a quadrangular pyramid form with a depth smaller than a thickness of the semiconductor substrate from the first surface side of the semiconductor substrate by anisotropic etching for the plurality of photodiodes; a third step of forming a vertical hole substantially perpendicular to the second surface by dry etching from the second surface side at a position corresponding to the pyramidal depression, and connecting the pyramidal depression to the vertical hole, so as to form a through hole penetrating through the semiconductor substrate from the second surface to the first surface; and a fourth step of forming a conductive

layer extending from the second surface to the first surface by way of the through hole.

[0012]

In this method, the vertical hole is formed after the pyramidal depression having a quadrangular pyramid form is formed. Thus formed pyramidal depression has a depth smaller than the thickness of the semiconductor substrate. As a consequence, etching solutions do not leak to the second surface side, and thus do not adversely affect the photodiodes on the second surface side.

[0013]

[Embodiments of the Invention]

In the following, embodiments of the present invention will be explained. Here, constituents identical to each other will be referred to with numerals identical to each other without repeating overlapping descriptions.

Fig. 1 is a plan view enlarging a part of the photodiode in accordance with a first embodiment, whereas Fig. 2 is a sectional view thereof.

[0014]

In the following explanation, the surface on which light is incident will be referred to as front side, whereas the surface opposite therefrom will be

referred to as rear side. In the photodiode array 1 of this embodiment, a plurality of pn junctions 4 are regularly arranged in an array of a matrix on the front side, each pn junction functioning as a photo-sensitive pixel of the photodiode array 1. The photodiode array 1 comprises an n-type silicon substrate 3 having a thickness of 270 μm and an impurity concentration of 1×10^{12} to $10^{15}/cm^3$; and a plurality of p-type impurity diffusion layers 5 arranged with a pitch of about 1.5 mm, each having a size of 500 μm × 500 μm, a depth of 0.5 to 1 μm in the substrate, and an impurity concentration of 1×10^{13} to $10^{20}/cm^3$. The photo-sensitive pixels are constituted by the pn junctions 4 formed between the n-type silicon substrate 3 and a plurality of p-type impurity diffusion layers 5. An n^+-type impurity area (separation layer) 7 for separating the photodiodes from each other and trapping unnecessary carriers so as to reduce dark currents is disposed between the p-type impurity diffusion layers 5.

[0015]

A first hole part 11 (vertical hole part) and a second hole part 13 (pyramidal hole part) are formed on the front and rear sides, respectively, between the pn junctions 4 adjacent to each other. Fig. 3 shows views of through hole 12 formed by connecting a first

hole part 11, a second hole part 13, and Fig. 3(a) is a plan view of the through hole 12, and Fig. 3(b) is a III-III sectional view thereof, and Fig. 3(c) is a perspective view thereof. The first hole part 11 is formed with a diameter of 10 μm on the front side of the substrate so as to be substantially parallel to the thickness direction of the substrate. The first hole part 11 is formed like a cylinder substantially parallel to the thickness direction of the substrate at a position penetrating through the separation layer 7. The hole is formed with a depth not smaller than the depth by which the p-type impurity diffusion layer 5 is formed. This prevents the second hole part 13 from limiting the depletion layers extending from the pn junctions 4, whereby the p-type impurity diffusion layers 5 can be arranged close to each other.

[0016]

The second hole part 13 is formed like a quadrangular pyramid from the rear side of the substrate, with its width tapering down toward the front side. The second hole part 13 is formed by anisotropic etching from the rear side, whereby a (111) plane is exposed at the wall surface of the hole part, and the wall surface forms an angle of about 54.7° with respect to the surface of the photodiode array (angle $\alpha \approx 54.7°$ in Fig. 3(b)). Since the second

hole part 13 is formed like a quadrangular pyramid, it is easier to provide the inner wall of the hole part with a conductive layer (through hole wiring).

[0017]

The first hole part 11 and second hole part 13 are connected to each other within the substrate, so as to form a single through hole 12. The front and rear sides of the substrate, including the wall surface of the through hole 12 and the front side of the p-type impurity diffusion layers 5, are covered with a thermally oxidized layer 9 of silicon. Not only the thermally oxidized silicon layer but also an AR coat may be formed according to a required wavelength sensitivity of photodiodes. The AR coat may be a single layer of any of SiO_2 and SiNx, or an insulator composite film or laminated film including them.

[0018]

A through hole wiring 17 is formed by aluminum on the thermally oxidized layer 9, and is in contact with the p-type impurity diffusion layer 5 by way of a contact hole 15 formed in the thermally oxidized layer 9. Further, the through hole wiring 17 extends to the rear side by way of the wall surface of the through hole 12, so as to be able to come into electric contact with the p-type impurity diffusion layer 5

from the rear side. Here, there will be no problems even if the first hole part 11 is filled with the metal of the through hole wiring 17 so that the front and rear sides of the substrate are spatially separated from each other, since the electric contact between the p-type impurity diffusion layer 5 and the rear side will not be lost (see Fig. 4). The material for the through hole wiring 17 is not limited to aluminum. Copper, nickel, gold, tungsten, titanium, polysilicon, and the like, or alloys or laminated metals including them may be used as well. In place of the thermally oxidized layer 9, an oxide film made by CVD may also be used. An oxide or nitride film made by CVD may also be disposed between the thermally oxidized layer 9 and through hole wiring 17. This can secure a high insulating property between the silicon substrate and the through hole wiring 17.

[0019]

Further, in this photodiode array, the through hole 12 is filled with a filler material 10 such as a resin on the through hole wiring 17) (see Fig. 5). Though the front and rear sides of the substrate are spatially separated from each other thereby, the mechanical strength of the photodiode array 1 can be improved without losing the electric contact between the p-type impurity diffusion layer 5 and the rear side.

Here, the material filling the through hole 12 may be resin type insulating materials including epoxy, polyimide, acrylic, silicone, and urethane resins, or electrically conductive resins including an electrically conductive filler in addition to these insulating materials.

[0020]

In a similar way, the through hole 12 may be completely filled with a conductive material 10(see Fig. 6). The filling electrically conductive material not only improves the mechanical strength of the photodiode array 1, but may be used as a bump electrode as it is when projected in a hemispherical form from the hem of the second hole part 13 on the rear side. The electrically conductive material 10 may be solder, electrically conductive resins including electrically conductive fillers, and the like.

[0021]

In the following, a method of making the photodiode array whose through holes 12 are filled with a polyimide resin (see Fig. 5) will be explained. First, an n-type semiconductor (100) substrate 3 is prepared. The front side of the substrate is thermally oxidized, and a thermally oxidized layer 9, which is utilized as a mask for n^+ thermal diffusion

in the next step, is formed. At positions to become separation layers 7, the thermally oxidized film is bored by a photoetching process, and phosphorus is thermally diffused and thermally oxidized. Here, phosphorus is also diffused over the whole area of the rear side, whereby an n^+-type impurity concentration layer 19 is formed(see Fig.7).

[0022]

The thermally oxidizing layer is similarly bored at areas for forming pn junctions 4, and boron is thermally diffused and thermally oxidized. The areas of pn junctions 4 become parts corresponding to photosensitive pixels. Further, contact holes 15 are provided in p+ and n+ layers. A silicon nitride film (SiNx) 23 and the thermally oxidized layer 9 is formed on the rear side by plasma CVD or LP-CVD, and is eliminated by etching from areas for forming second hole parts 13. The areas for forming the second hole parts 13 are located at positions corresponding to the separation layers 7 on the rear side (see Fig. 8). Here, the areas for eliminating the silicon nitride film 23 has been designed beforehand so as to have such forms and sizes that the vertices of quadrangular pyramids of second hole parts 13 do not reach the front side upon alkali etching, which will be explained later, and are located at positions corresponding to

the separation layers 7 on the front side.

[0023]

The semiconductor substrate 3 is subjected to anisotropic etching with an alkali (e.g., potassium hydroxide solution, TMAH, hydrazine, or EDP) from the rear side, so as to form the second hole parts 13, while protecting the surface. Namely, the substrate is etched from the crystal plane (100), so as to expose the (111) plane. Each second hole part 13 is formed like a quadrangular pyramid by etching, whereas the etching automatically stops at the vertex of the quadrangular pyramid (see Fig. 9).

Etching may be stopped before reaching the vertex of the quadrangular pyramid as well. Next, the parts corresponding to the vertices of thus formed quadrangular pyramids are dry-etched from the front side, so as to form first hole parts 11, which are further etched until they connect with the vertices of quadrangular pyramids of second hole parts 13, so as to form through holes 12 constituted by the first hole parts 11 and second hole parts 13. The n^+ layers 25 surrounding their corresponding through holes 12 are formed by ion implantations or diffusions from the rear side(see Fig. 10).

[0024]

The n^+ layers 25 connect with the separation

layers 7 and the n^+-type impurity concentration layers 19 on the rear side. Thereafter, for securing insulation of side walls, SiO_2 layers 27 are formed by thermal oxidization). The insulating layers for side walls may be not only the SiO_2 layers 27, but also laminate films with SiNx, SiO_2 films formed by CVD, and the like. Next, aluminum is deposited from both sides by a sputtering apparatus in order to form the through hole wirings 17 and a resist is formed by etching so as to form a desired pattern. The material for the through hole wirings 17 is not limited to aluminum, whereas the method of forming the wirings is not limited to sputtering. For example, a polysilicon part formed by CVD may be subjected to diffusion for lowering the electric resistance. In this case, only the contact hole parts may be made of aluminum and electrically connected to the polysilicon part.

[0025]

A photosensitive polyimide layer 29 is formed on the rear side, and is bored only at locations where bump electrodes 33 are to be disposed. Then, the bump electrodes 33 are formed by way of under bump metal 37 (hereinafter referred to as "UBM") parts formed by a metal establishing an electrically/physically excellent connection to the bump electrodes 33. When

the bump electrodes 33 are solder bumps, for example, wettable metal parts should be formed between solder and aluminum, since solder is not wettable with aluminum. The UBM parts in this case can be realized by forming Ni-Au by electroless plating or forming Ti-Pt-Au or Cr-Au by lift-off procedure. An acrylic layer, an epoxy layer, and a layer of a composite material including them may also be used in place of the polyimide layer. The solder bumps can be formed by disposing solder at predetermined UBM parts by a solder ball mounting method or a printing method, and then causing thus disposed solder to reflow. The bump electrodes 33 are not limited to solder bumps, but may be electrically conductive bumps including metals such as gold bumps, nickel bumps, copper bumps, and conductive resin bumps(see Fig. 11).

[0026]

Though the n-type semiconductor substrate is initially prepared, and an n^+-type impurity concentration layer is formed by thermal diffusion in the above-mentioned method, an n-type semiconductor substrate provided with an n^+-type impurity concentration layer beforehand by thermal diffusion or epitaxial growth may be prepared. This can increase the thickness of the n^+-type impurity concentration layer in the photodiode array as shown

in Fig. 12, so that the distance between the substantially p-type impurity diffusion layer 5 and the n^+-type impurity concentration layer 19 can be short. As a consequence, the resistance component can be reduced, whereby the response can be fast. Also, regulating the distance between the substantially p-type impurity diffusion layer 5 and the n^+-type impurity concentration layer 19 can yield spectral sensitivity curve characteristics conforming to given specifications.

[0027]

Effects of the above-mentioned photodiode array and method of making the same will now be explained. In the above-mentioned photodiode array, the second hole parts 13 are initially formed by alkali etching from the rear side, and then the first hole parts 11 are formed, whereby the through holes 12 are formed. Thus, the through holes are not completed at the time of alkali etching step, whereby no erosion toward the front side is caused by alkali etching. Since the photosensitive surface is not adversely affected in particular, the yield can be prevented from decreasing.

[0028]

In the alkali etching step, the etching is stopped when each second hole part 13 is etched to the

vertex of its quadrangular pyramid. Thus, there is no need for separately providing an etching stop layer or the like. Since a major part (second hole part 13) of each through hole 12 is formed by anisotropic etching, unevenness is smaller in the wall surface, whereby the smooth wall surface can be obtained in the through hole. Therefore, unnecessary carriers are restrained from occurring because of damages in the wall surface of the through hole, whereby dark currents can be reduced.

[0029]

Fig. 13 shows schematic sectional views of the portion around through hole 12 in a photodiode array. The wall surface of the second hole part 13 forms an angle of 54.7° with respect to the array direction of the photodiode array, whereas the wall surface of the first hole part 11 is substantially perpendicular to the array direction. When a through hole is formed by the second hole part 13 alone by using alkali etching, the second hole part and the front side of the photodiode array directly connect with each other, whereby the angle θ formed between their surfaces becomes acute(see Fig. 14). In the above mentioned photodiode array, as shown in Fig. 13(a), by contrast, the through hole 12 is formed by connecting two hole parts to each other, whereby the angle B formed at

their junction is 90° or greater. Further, the angle A formed between the second hole part 13 and the rear side of the photodiode is 90° or greater, whereas the angle C formed between the first hole part 11 and the front side of the photodiode is about 90°. Therefore, the through hole wiring 17 extending from the front side to the rear side by way of the through hole 12 has no part bent by an acute angle, and thus can restrain conduction from failing because of insufficient coverage at the time of forming. Further, depending on the dry-etching condition at the time of making the first hole part 11, the first hole part 11 may be tapered, so as to form an angle C of 90° or greater as shown in Fig. 13(b). This can further restrain conduction from failing.

[0030]

Since the second hole part 13 in the photodiode is formed by alkali etching, ions can be implanted into the wall surface of the through hole 12, whereby the n^+ layer 25 can easily be formed by ion implantation. Thus formed n^+ layer 25 acts as a separation layer for separating the photodiodes from each other, and traps unnecessary carriers so as to reduce dark currents.

[0031]

In the photodiode array, the first hole part 11 is formed so as to penetrate through the separation

layer 7. Therefore, even when the inner wall of the first hole part 11 is damaged and so forth at the time of dry etching for forming the hole part, generated unnecessary carriers are trapped by the separation layer 7. Hence, the photodiode array can prevent leak currents and the like from occurring because of damages when forming through hole wirings.

[0032]

[Effects of the Invention]

As explained in the foregoing, the present invention can provide a photodiode array which is less likely to cause conduction failures in through hole wirings, while yielding a high fill factor.

[Brief Description of the Drawings]

[Fig. 1]

A plan view of the photodiode array in accordance with a first embodiment;

[Fig. 2]

A sectional view of the photodiode array in accordance with the first embodiment;

[Fig. 3]

(a) is a plan view of a through hole, and (b) is a III-III sectional view, (c) is a perspective view.

[Fig. 4]

A sectional view of a photodiode;

[Fig. 5]

A sectional view of a photodiode;

[Fig. 6]

A sectional view of a photodiode;

[Fig. 7]

A sectional view of a photodiode for explaining a manufacturing step thereof;

[Fig. 8]

A sectional view of the photodiode for explaining a manufacturing step thereof;

[Fig. 9]

A sectional view of the photodiode for explaining a manufacturing step thereof;

[Fig. 10]

A sectional view of the photodiode for explaining a manufacturing step thereof;

[Fig. 11]

A sectional view of the photodiode for explaining a manufacturing step thereof;

[Fig. 12]

A sectional view of a photodiode;

[Fig. 13]

Sectional views of a photodiode;

[Fig. 14]

A sectional view of a photodiode.

[Explanation of Reference Numerals]

1…photodiode array、3…substrate, 4…pn-junction、

5…p-type impurity diffusion layer, 7…separation layer, 9…thermal oxidation film, 10…filler material, 11…first hole part、12…through hole、13…second hole part, 15…contact hall, 17…through hole wiring, 19…n^+type impurity concentration layer、23…silicon nitride film,29…photosensitive polyimide layer, 33…bump electrode.

[Document Name] ABSTRACT

[Abstract]

[Problem] A photodiode array which is less likely to cause conduction failures in through hole wirings, while yielding a large fill factor is provided.

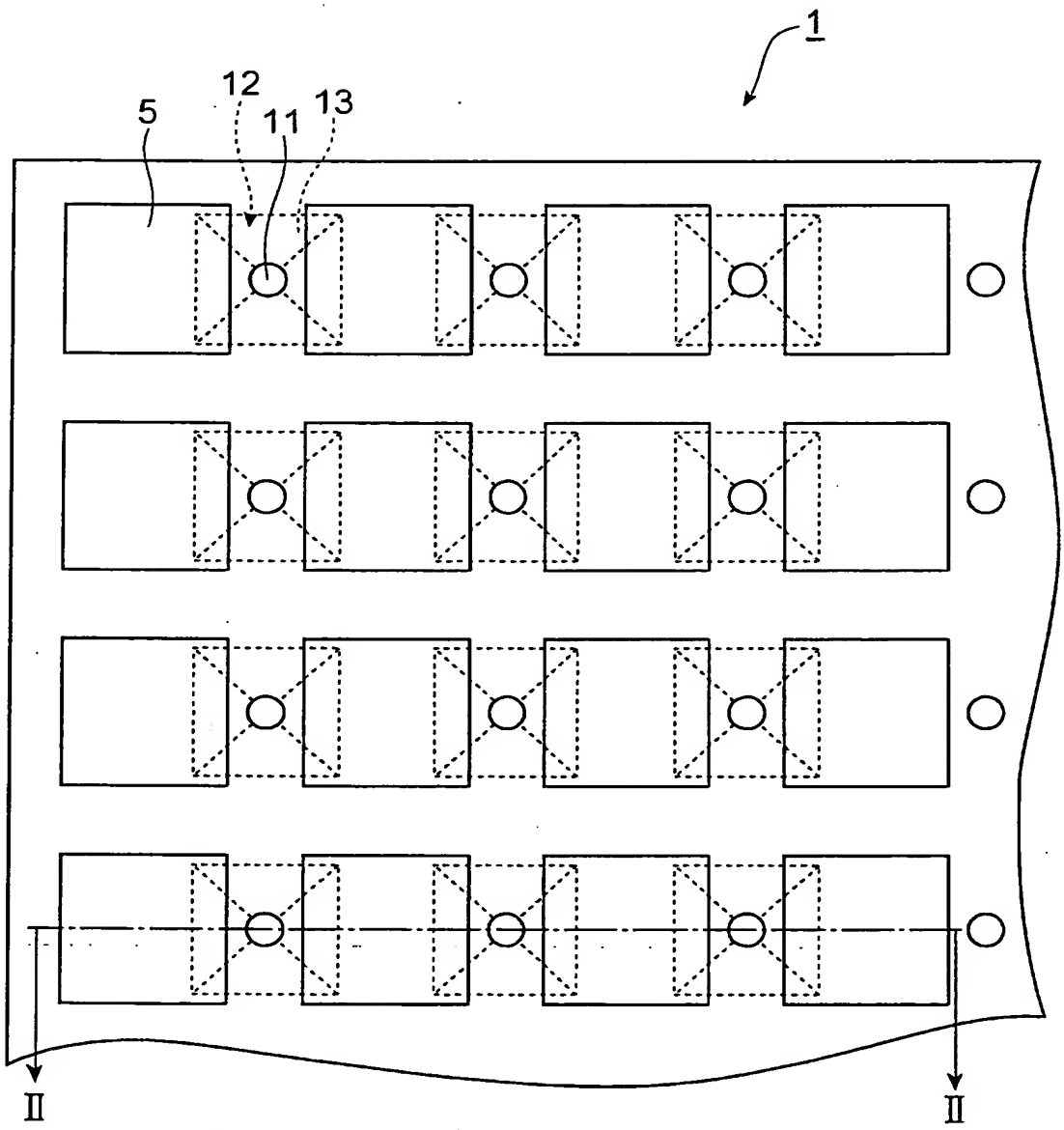
[Means of Solution]

A photodiode array comprises a semiconductor substrate formed with an array of a plurality of pn junction type photodiodes on a light incident surface side, the surface opposite from the incident surface in the semiconductor substrate being made of a (100) plane; a through hole, formed in an area held between the photodiodes, penetrating through the semiconductor substrate from the incident surface side to the opposite surface side; and a conductive layer extending from the incident surface to the opposite surface by way of a wall surface of the through hole; the through hole being formed by connecting a vertical hole part formed substantially perpendicular to the incident surface on the incident surface side, and a pyramidal hole part formed like a quadrangular pyramid on the opposite surface side to each other within the semiconductor substrate; the pyramidal hole part having a wall surface formed as a (111) plane.

[Selected Drawing] Fig. 2

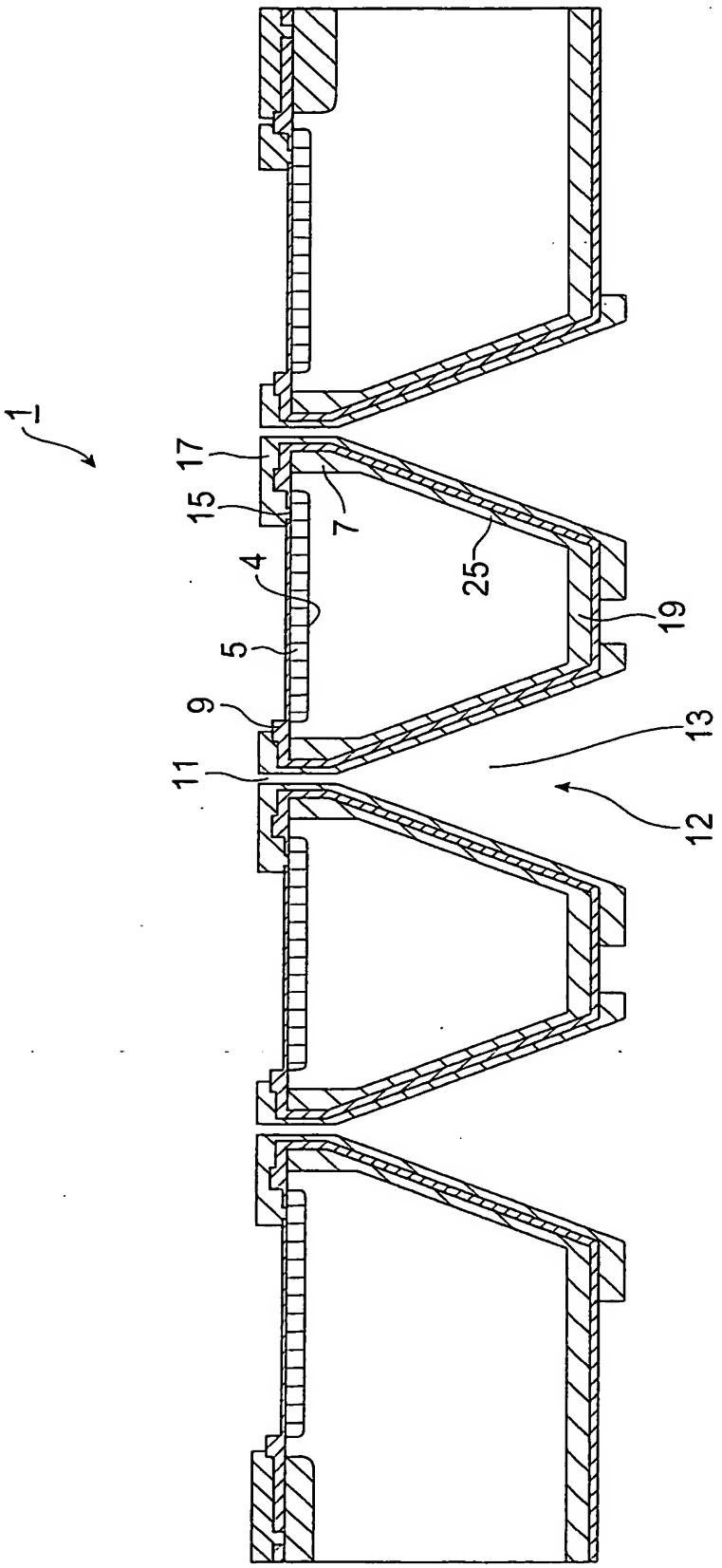
【書類名】DOCUMENT ~~図面~~ DRAWING
NAME

【~~図~~1】
Fig.1



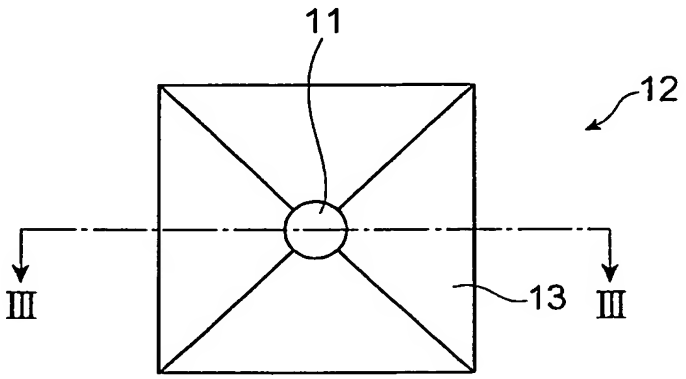
【図2】

Fig. 2



【図3】
Fig. 3

(a)



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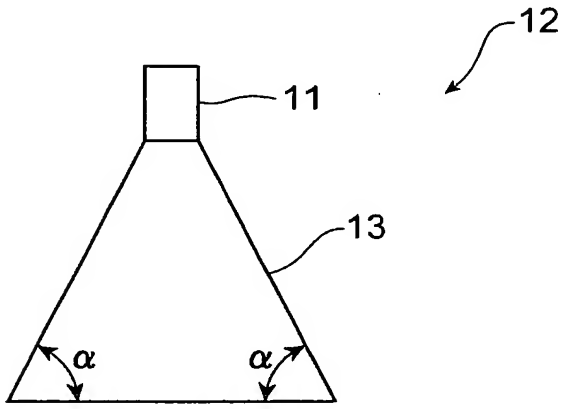

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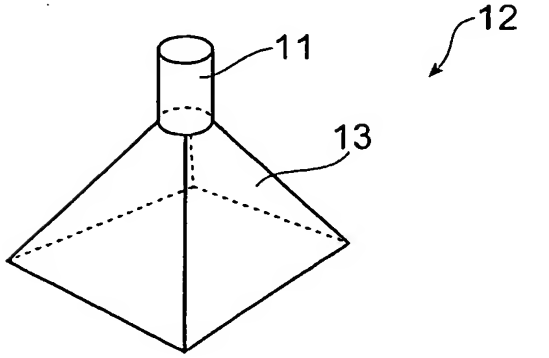
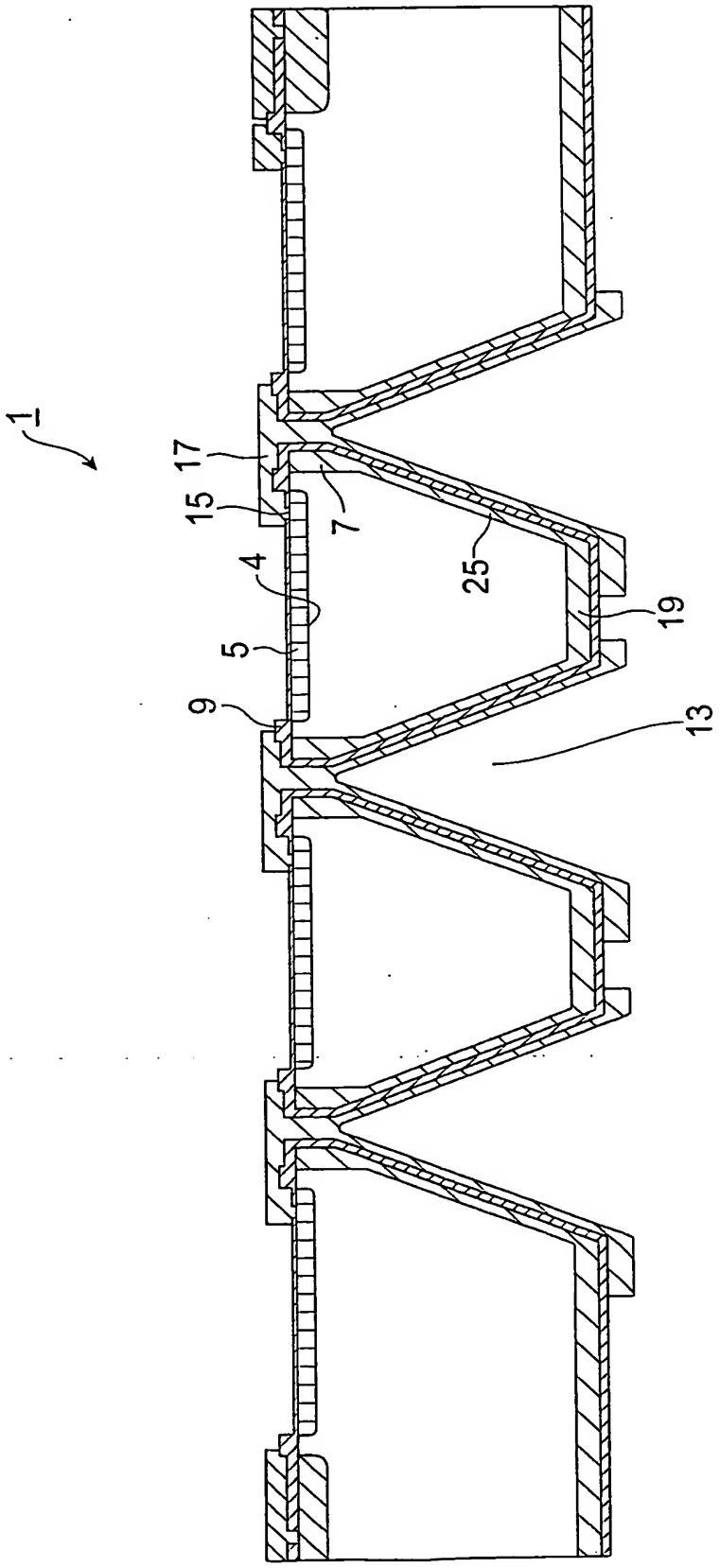
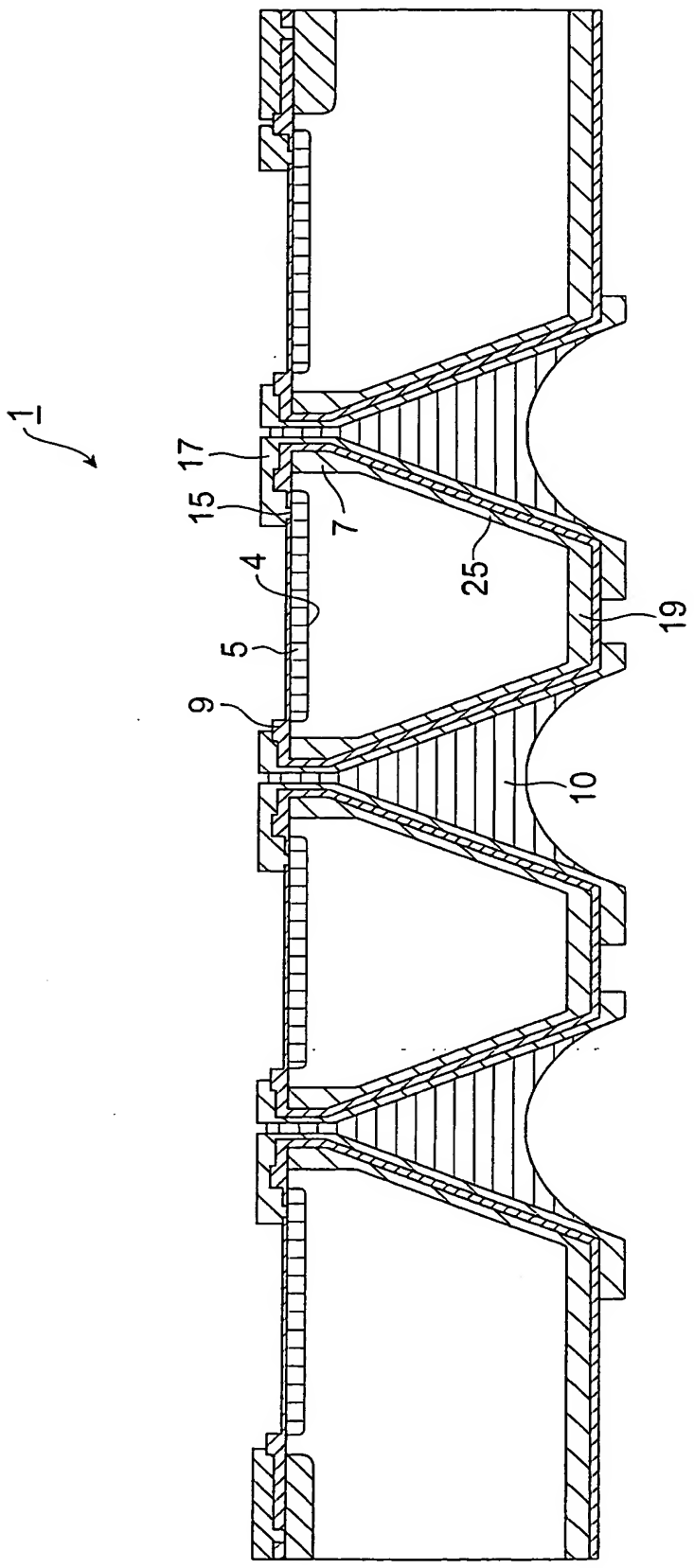


【図４】
Fig. 4

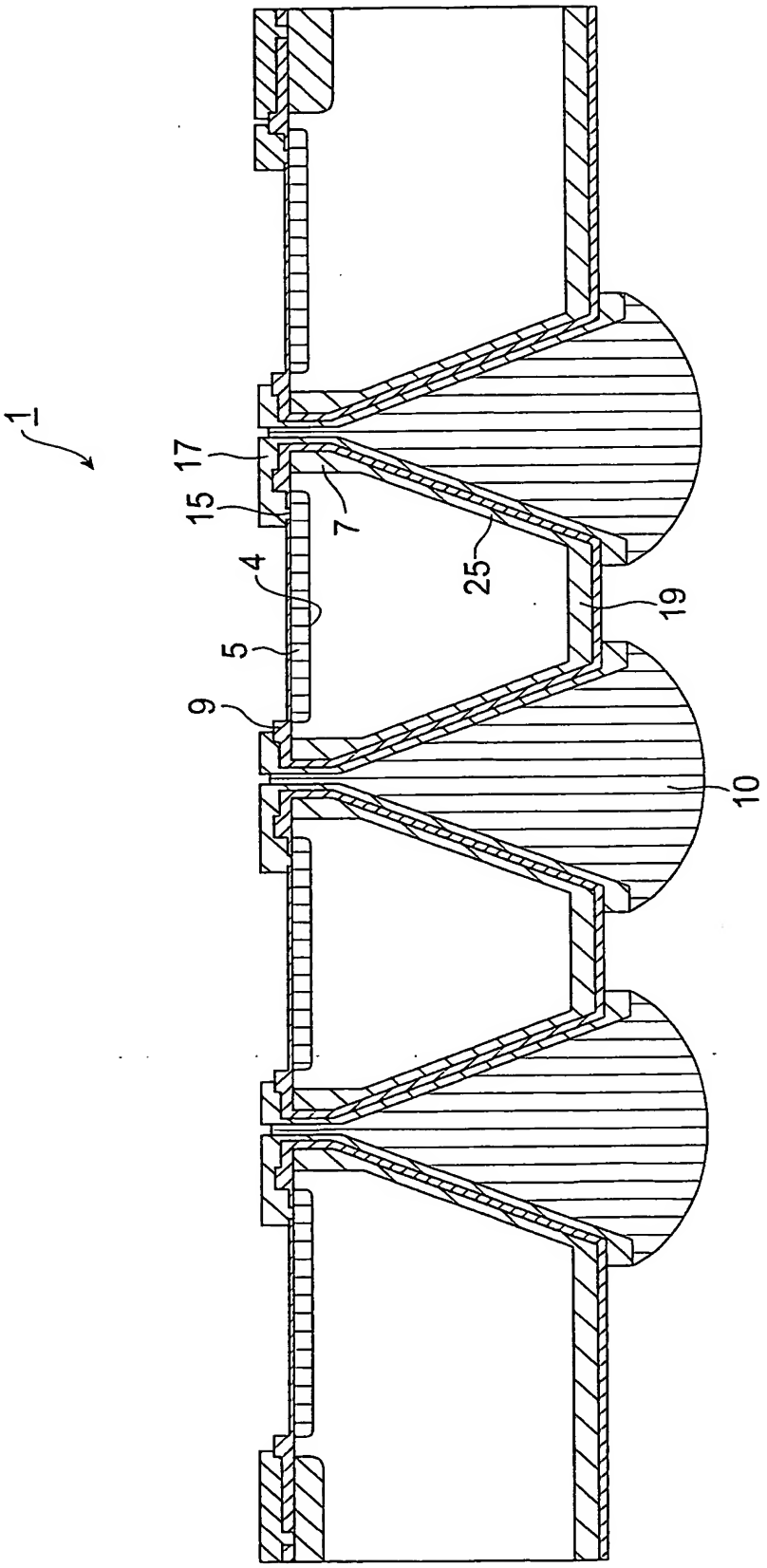


【図５】

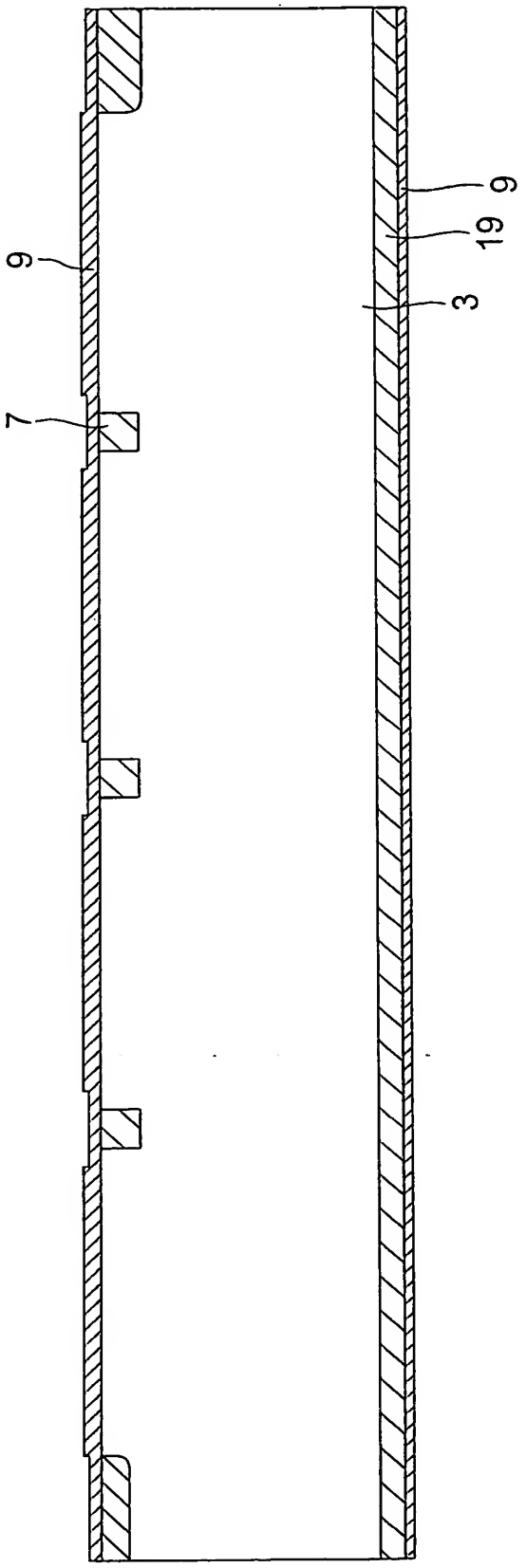
Fig.5



【図6】
Fig. 6

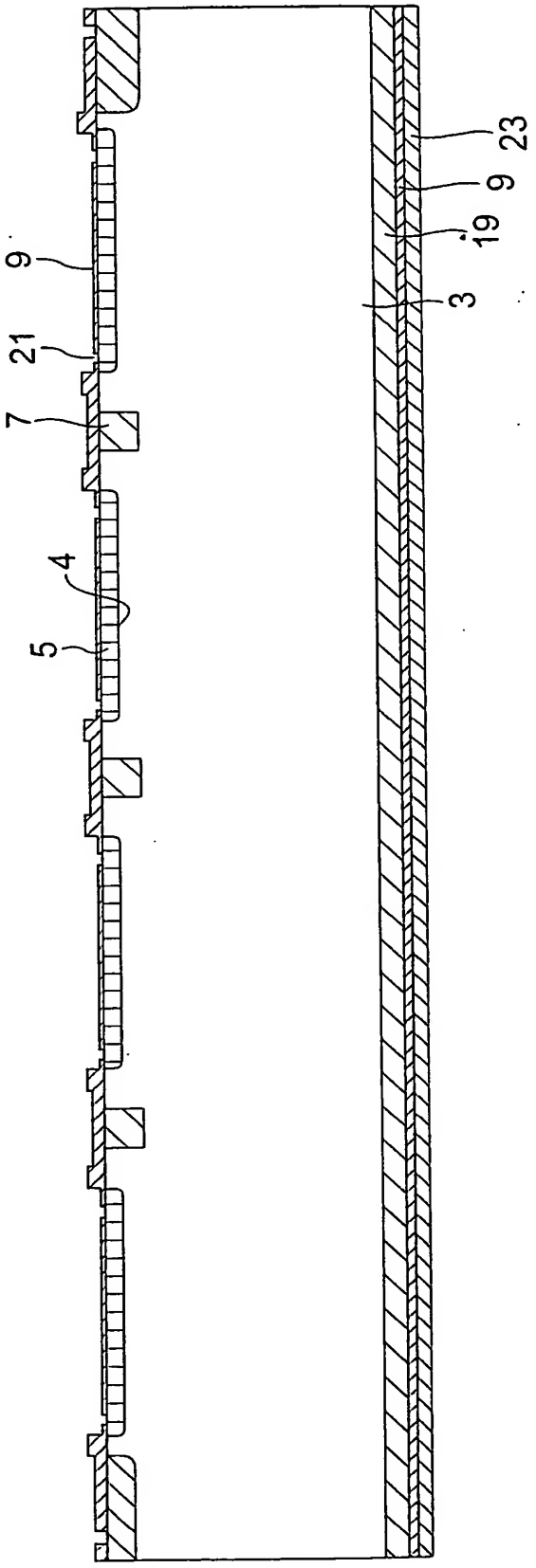


【図７】
Fig. 7

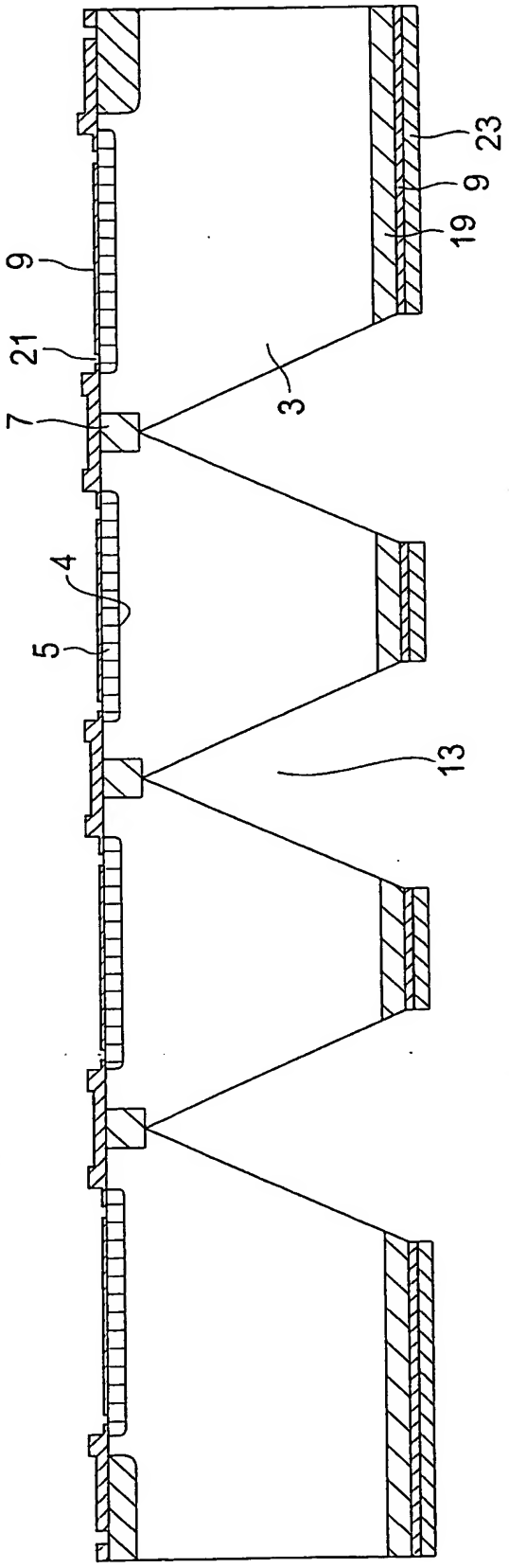


【図8】

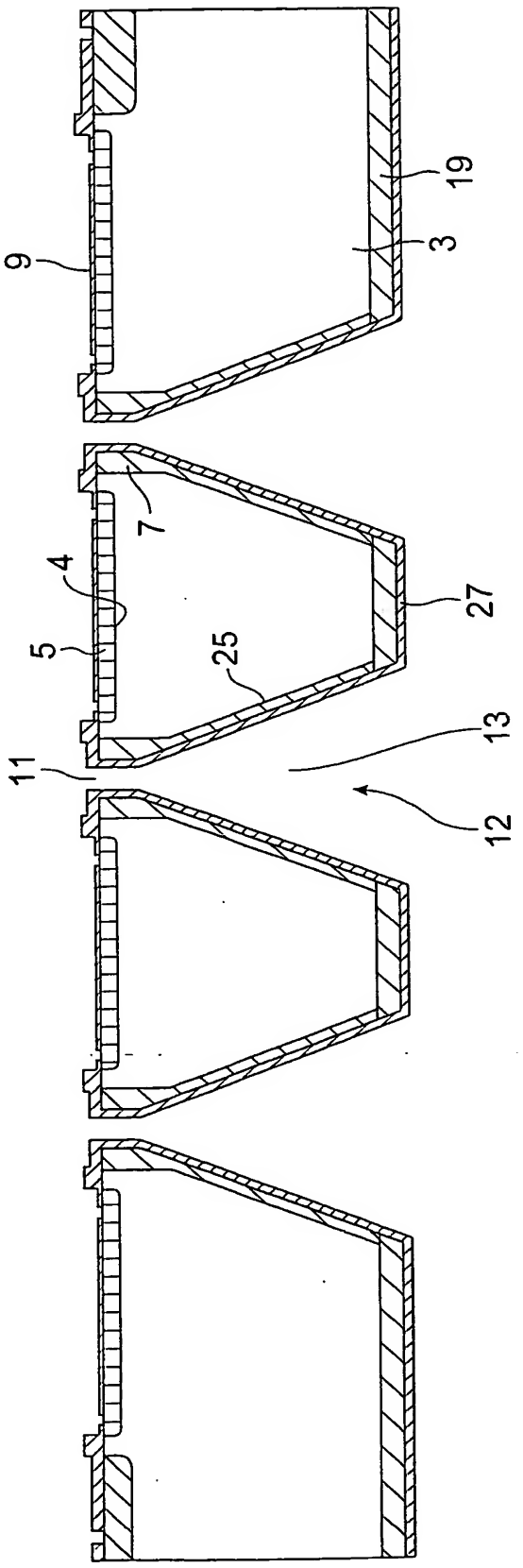
Fig. 8



【図９】
Fig. 9

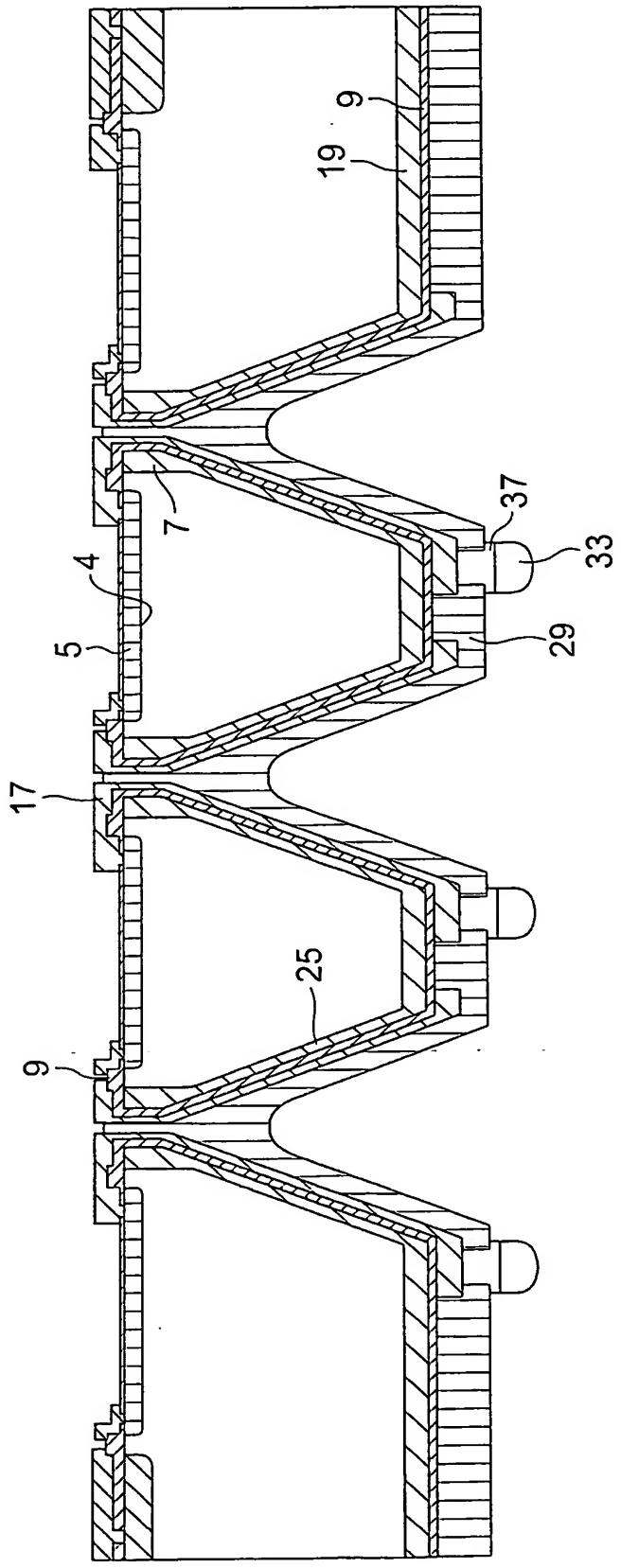


【図１０】
Fig. 10



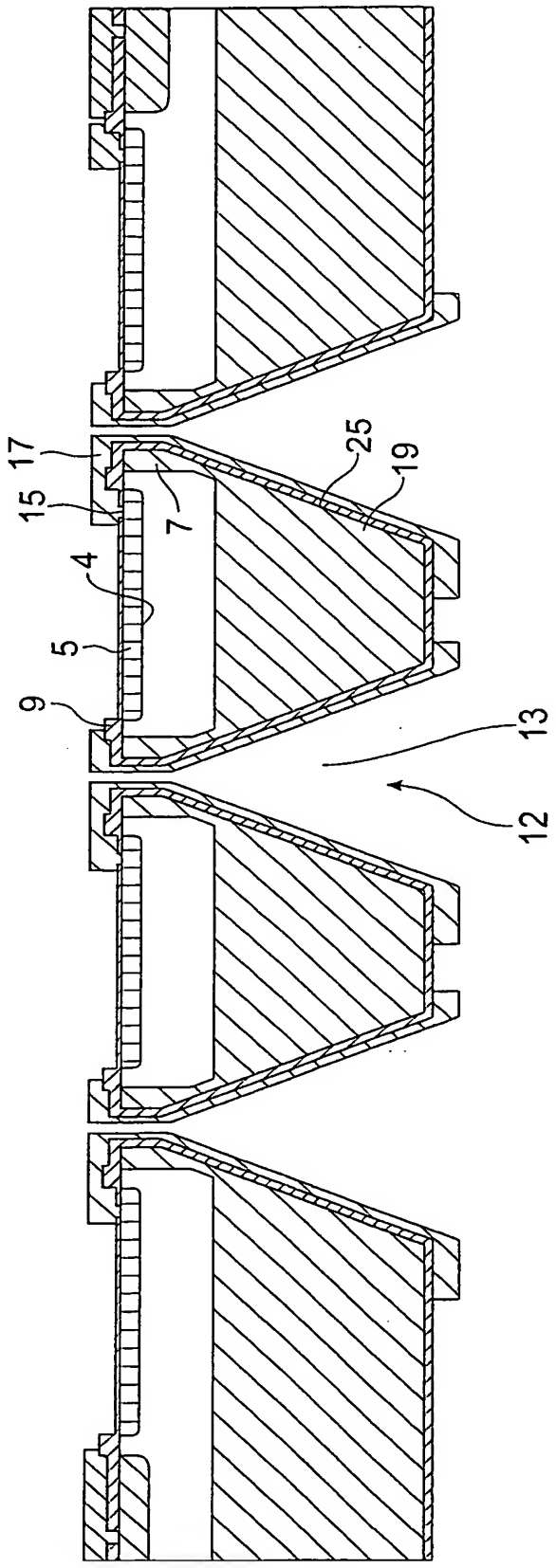
【図１１】

Fig. 11



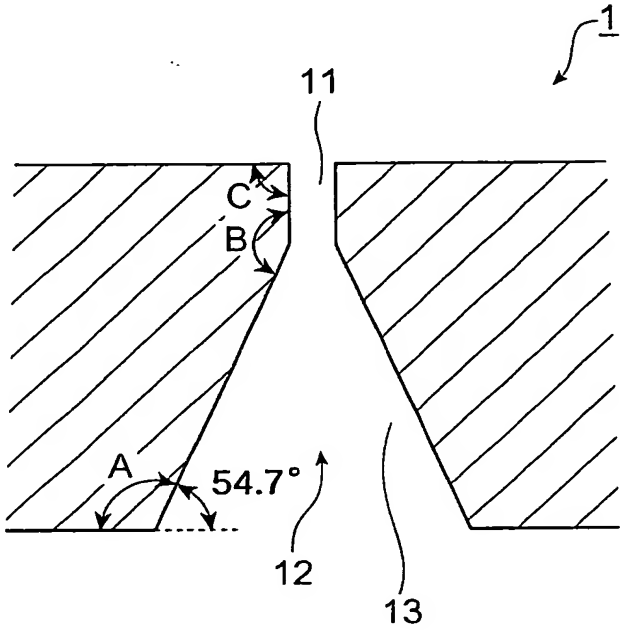
【図１２】

Fig. 12

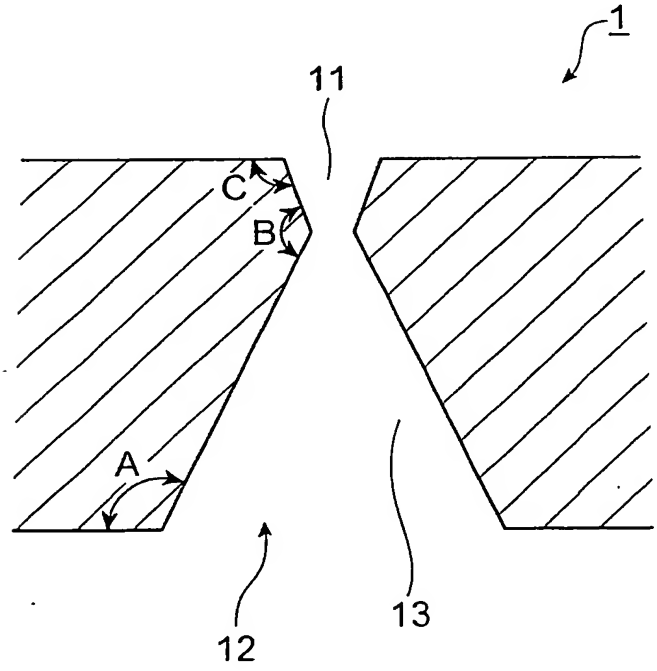


【図１３】
Fig. 13

(a)



(b)



【図１４】

Fig. 14